AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit (IC) comprising:

a clock distribution grid distributing a clock to local circuits, said distribution grid having a known load capacitance;

a clock driver driving said clock distribution grid;

at least one inductor connected at one end to said distribution grid, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor, wherein said clock driver is driving a first clock phase, said one end of said at least one inductor being connected to said first clock phase;

a second clock phase, said at least one inductor being connected to said second phase at an other end, said local grid capacitance comprising local wiring capacitance from both of said first clock phase and said second clock phase; and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor.

2. (original) An IC as in claim 1, wherein said at least one inductor is connected to a decoupling capacitor (decap) at an other end.

3. (original) An IC as in claim 2, wherein a voltage develops across each said decap, said voltage being midway between a high level and low level of said clock.

4. (original) An IC as in claim 3, wherein said decap is a pair of decaps, a first of said pair being connected between a first supply line and said other end of said inductor and an other of said pair being connected between said other end and a second supply line.

5. (original) An IC as in claim 4, wherein said second supply line is a ground line.

6. (previously presented) An IC as in claim 1, wherein said power grid lines include supply and supply return lines terminating on endpoints of a fingered gap pattern in the immediate vicinity of said at least one inductor.

7. (original) An IC as in claim 1, wherein said at least one inductor is four inductors located in four quadrants around said clock driver.

8 – 12 (canceled)

13. (currently amended) An IC assembly as in claim 28 [[12]], wherein said at least one inductor is connected to a decoupling capacitor (decap) at an other end.

14. (original) An IC assembly as in claim 13, wherein a voltage develops across each said decap, said voltage being midway between a high level and low of said clock.

15. (original) An IC assembly as in claim 14, wherein said decap is a pair of decaps, a first of said pair being connected between a first supply line and said other end of said inductor and an other of said pair being connected between said other end and a second supply line.

16. (currently amended) An IC assembly as in claim 15, wherein said second supply line is a ground line, both said first supply line and said ground line terminating on endpoints of a fingered gap pattern.

17. (canceled)

18. (previously presented) An IC assembly as in claim 28, further comprising:

a pair of cross coupled inverters connected between said first clock phase and said second clock phase.

19. (previously presented) An IC assembly as in claim 28, further comprising a second clock driver driving said second clock phase.

20. (currently amended) An IC assembly as in claim 28 [[12]], wherein said at least one inductor is four inductors located in four quadrants around said clock driver.

21 – 27 (canceled)

28. (previously presented) An integrated circuit (IC) assembly clocked by a global clock, said global clock being distributed to a plurality of sectors, each of said sectors comprising:

a clock distribution grid distributing a sector clock to local circuits, said distribution grid having a known load capacitance;

a clock driver driving said clock distribution grid;

at least one inductor connected at one end to said distribution grid, said clock having a frequency within the frequency range of the resonant frequency of local grid capacitance and said at least one connected inductor, wherein said clock driver is driving a first clock phase, said one end of said at least one inductor being connected to said first clock phase;

a second clock phase, said at least one inductor being connected to said second phase at an other end, said local grid capacitance comprising local wiring capacitance from both of said first clock phase and said second clock phase; and

a power grid, power grid lines being discontinuous in the vicinity of each said at least one inductor, whereby power grid line loops are open in the vicinity of each said at least one inductor.